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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/821,901	04/09/2004	Koji Imai	501646.20004	2446

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EXAMINER	
FIDLER, SHELBY LEE	
ART UNIT	**PAPER NUMBER**
2861	

DATE MAILED: 03/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/821,901	IMAI, KOJI	
	Examiner	Art Unit	
	Shelby Fidler	2861	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-12 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-4 and 6-12 is/are rejected.

7)☒ Claim(s) 5 is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 09 April 2004 is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 7/23/2004.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4 and 6-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Imai et al. (JP 2000158643) in view of Ghozeil et al. (US 6375295 B1).

Imai teaches the following:

***regarding claim 1**, a driving apparatus for at least one recording head, the apparatus comprising:

a first waveform signal receiver (*wave generating circuit*) that receives through signal lines (*par. 15, lines 4-5*), a plurality of waveform signals (*par. 15, lines 4-5*) representing various recording modes (*par. 8, lines 5-8*);

a first drive signal provider (*1st selection means 33 from the bottom of circuit 21, Figure 3*) that generates drive signals on the basis of the plurality of waveform signals received by the first waveform signal receiver (*par. 8, lines 2-4*), and supplies the drive signals to one of recording element groups included in the at least one recording head (*par. 29, lines 2-5 with 1st selection means respective driver 34, Figure 3*);

a second drive signal provider (*2nd selection means 33 from the bottom of circuit 21, Figure 3*) that generates drive signals of the basis of waveform signals (*par. 8, lines 2-4*), and supplies the

drive signals to another recording element group (*par. 29, lines 2-5 with 2nd selection means respective driver 34, Figure 3*);

***regarding claim 2**, the number of recording element groups is N that is a natural number of two or more (*64 channels, Figure 3*), and the apparatus comprises:

N drive signal providers (*selection means 33*), including the first and second drive signal providers (*a selection means 33 for each respective channel, Figure 3*), each of which generates drive signals on the basis of either the plurality of waveform signals received by the first waveform signal receiver (*par. 8, lines 2-4*) or the waveform signals delayed by a corresponding one of the (N-1) delay circuits, and supplies the drive signals to a corresponding one of the recording element groups (*par. 29, lines 2-5 with selection means respective driver 34, Figure 3*)

***regarding claim 3**, the number of recording element groups is N that is a natural number of three or more (*64 channels, Figure 3*), and the apparatus comprises:

third to Nth drive signal providers (*If N=64, channels 0-61, Figure 4*) each of which generates drive signals on the basis of the waveform signals (*par. 8, lines 2-4*), and supplies the drive signals to another recording element group (*par. 29, lines 2-5 with selection means respective driver 34, Figure 3*)

***regarding claim 4**, N is four or more (*N=64 channels, Figure 3*)

***regarding claim 7**, each of the first and second drive signal providers receives image data (*par. 45, lines 9-10*) for recording elements of a corresponding one of the recording element groups (*par. 47, lines 1-3*), and selects one of the plurality of waveform signals on the basis of the image data (*par. 48, lines 6-9*) so as to generate and supply a drive signal to each of the recording elements of the corresponding group (*par. 49, lines 1-3*)

***regarding claim 8**, each of the plurality of waveform signals is for forming one dot (*Figure 7 shows the different waveforms, each forming a single dot*), and the waveform signals differ from each other in at least one of the number of pulses, pulse width, and pulse height (*Figure 7 shows that the waveforms signals differ in number of pulses*)

***regarding claim 9**, each of the plurality of waveform signals is for forming one dot (*Drawing 7 shows each of the three waveforms, and their respectively formed dots*), and dots formed from the plurality of waveform signals are different from each other in tone (*par. 50, lines 10-11*)

***regarding claim 10**, an image recording apparatus comprising:

waveform signal generators (*elements 35a/b/c, Figure 4*) that generates a plurality of waveform signals representing various recording modes (*par. 54, lines 5-7*);

at least one recording head (*printhead 3, Figure 1*) including a plurality of recording element groups (*those groups associated with drivers 34, Figure 4*); and

a driving apparatus that drives the at least one recording head (*drive circuit 21, Figure 4*);

the driving apparatus comprising:

a first waveform signal receiver (*bottom-most selection means 33 of circuit 21 acts as a first waveform receiver, Figure 4*) that receives, through signal lines (*signal lines between waveform generators 35 and bottom most selection means 33, Figure 4*), the plurality of waveform signals received by the first waveform signal generator (*waveform generators 35, Figure 4*), and supplies the drive signals to one of the recording element groups included in the at least one recording head (*group corresponding to channel 63, Figure 4*);

a second drive signal provider (*selection means 33 corresponding to channel 62, Figure 4*) that generates drive signals on the basis of the waveform signals (*par. 8, lines 2-4*) and supplies

the drive signals to another recording element group (*par. 29, lines 2-5 with 2nd selection means respective driver 34, Figure 3*)

***regarding claim 11**, an image data generator (*inherent with existence of image data, par. 41, lines 1-4*) that outputs, to each of the first and the second drive signal providers, image data for recording elements of a corresponding one of the recording element groups (*par. 54, lines 5-7*), wherein each of the first and second drive signal providers selects one of the plurality of waveform signals on the basis of the image data (*par. 8, lines 2-4*) so as to generate and supply a drive signal to each of the recording elements of the corresponding group (*par. 29, lines 2-5 with 1st selection means respective driver 34, Figure 3*)

***regarding claim 12**, the waveform signal generator generates the plurality of waveform signals repeatedly in constant printing cycles (*par. 48, lines 1-4*)

Imai et al. do not expressly teach the following:

***regarding claim 1**, a first delay circuit that delays the waveform signals received by the first waveform signal receiver; and

drive signals are generated on the basis of the waveform signals delayed by the first delay circuit

***regarding claim 2**, (N-1) delay circuits, including the first delay circuit, connected to each other in series, each of the delay circuits sequentially delays the waveform signals delayed by the first delay circuit

***regarding claim 3**, second to (N-1)th drive circuits connected to the first delay circuit, the second to (N-1)th delay circuits further delaying the waveform signals delayed by the first delay circuit; and

third to Nth drive signal providers receive waveforms delayed by a corresponding one of the (N-2) delay circuits

***regarding claim 4**, the second to (N-1)th delay circuits are connected to each other in series

***regarding claim 6**, the degree of delay of the waveform signals by the first delay circuit is changeable

***regarding claim 10**, a single waveform signal generator that generates a plurality of waveform signals; a first delay circuit that delays the waveform signals received by the first waveform signal receiver, and sending those delayed waveform signals to the second drive signal provider. At the time of invention, it would have been obvious to a person of ordinary skill in the art to integrate the multiple waveform signal generators into a single waveform signal generator, since it has been held that constructing a formerly integral structure in various elements involves only routine skill in the art. Nerwin v. Erlichman, 168 USPQ 177, 179. The motivation for doing so, is to reduce the number of parts.

Ghozeil et al. teaches the following:

***regarding claim 1**, a first delay circuit (*element 56*) that delays the waveform signals received by the first waveform signal receiver (*element 56 delays the original firing signal, Figure 3*);

drive signals are generated on the basis of the waveform signals delayed by the first delay circuit (*col. 3, lines 38-42*)

***regarding claim 2**, (N-1) delay circuits (*elements 56, 57, 58, etc., Figure 3*), including the first delay circuit (*col. 3, lines 38-42 shows that there are delay elements between each cell, so that there will be one less delay circuit than cells*), connected to each other in series (*elements 56, 57, 58, etc.*

connected in series, Figure 3), each of the delay circuits sequentially delays the waveform signals delayed by the first delay circuit (*col. 3, lines 38-42 with Figure 4*)

***regarding claim 3**, second to (N-1)th drive circuits (*cells 51*) connected to the first delay circuit (*for the purpose of this rejection, N=4 and cells 51B-D are connected to first delay circuit 56, Figure 3*), the second to (N-1)th delay circuits further delaying the waveform signals delayed by the first delay circuit (*col. 3, lines 54-57 with Figure 4 shows that each cells firing signal is delayed in series*); and

third to Nth drive signal providers (*logic select 40 corresponding to cell 51B*) receive waveforms delayed by a corresponding one of the (N-2) delay circuits (*cell 51B receives waveform data from the N-2 delay circuit 56, Figure 3*)

***regarding claim 4**, the second to (N-1)th delay circuits are connected to each other in series (*all delay circuits 56, 57, 58, etc. are connected in series, Figure 3*)

***regarding claim 6**, the degree of delay of the waveform signals by the first delay circuit is changeable (*col. 4, lines 18-27*)

***regarding claim 10**, a first delay circuit (*element 56*) that delays the waveform signals received by the first waveform signal receiver (*element 56 delays the original firing signal, Figure 3*), and sending those delayed waveform signals to the second drive signal provider (*col. 3, lines 38-42 shows that the firing signal is delayed from one cell to the next*)

Allowable Subject Matter

Claim 5 is objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Communication with the USPTO

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shelby Fidler whose telephone number is (571) 272-8455. The examiner can normally be reached on MWF 8:30-5:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Stephen Meier can be reached on (571) 272-2149. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

SLF

K. FEGGINS
PRIMARY EXAMINER